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The Effect of Body Doping On the Continuous Current of Junctionless Cylindrical Surrounding-Gate Nanowire Si-Mosfets



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Abstract

In the paper the effect of body doping on the continuous current of Junctionless Cylindrical Surrounding Gate-Nanowire Silicon Metal-Oxide-Silicon Field effect Transistors (MOSFETs) is presented. For accounting doping effect, we solved Poisson's Boltzmann equation including both types body doping and mobile charge concentrations, and obtained expressions for channel potential and Drain current (I_{DS}). Since, the junctionless transistor is a uniformly doped nanowire without junctions, has no doping concentration gradient in the channel. Thus JL SRG MOSFET has less fabrication steps and reduced operation complexity as compared to conventional MOSFET. The presented results are verified by comparing with Three Dimensional Simulation results of ref. [13] which shows reasonably good agreement. The proposed results in the analytical model of Nanowire SRG Si MOSFETs are valid for all the regions of operation.

Keywords: J L Nanowire SRG Si MOSFET, Poisson-Boltzmann's equation, body doping, mobile charge concentrations, channel potential and drain-current.

Introduction

In general, existing transistor are based on the use of semiconductor junctions. Because of laws of diffusion and statistical nature of the distribution of the doping atoms in the semiconductor, the formation of ultrashallow junctions with high doping concentration gradients has become a increasingly difficult challenge for industry. Overcome this challenge researchers are theoretically and experimentally proposed one more novel Field Effect Transistor, called Junctionless Cylindrical Surrounding Gate Nanowire Silicon Metal Oxide Semiconductor Silicon Field Effect Transistor (NWJL Si-MOSFET) [2-5]. Junctionless Metal Oxide-Silicon Field Effect Transistor (MOSFET) is a device without source/drain (S/D) junctions and extension regions. The JL Si MOSFETs can be realized by appropriately sizing the thickness of the silicon body with a proper doping concentration to control reasonable "ON" and "OFF" currents. The devices should be designed to have a fully depleted body in the subthreshold and accumulated regions when the transistors are turned "ON. The S/D in JL MOSFETs can be formed easily because of the S/D junction and body has the same doping type. It shows better short channel effects, less degradation mobility with temperature, small DIBL, subthreshold swing, and higher voltage gain which turn in good scalability below the 10nm and reduces fabrication complexity [9]. An analytically studies on double-gate (DG) JL MOSFET devices and the cylindrical nanowire (NW) MOSFET have been presented [6-10]. However, in the available models the influence of performance of Transistors with the variation of body doping concentration is not widely discussed. Therefore, still now we need to develop a simpler analytical model which brings faster and easier calculations. In this Paper, we proposed an analytical model for continuous current of JL SRG nanowire Si-MOSFETs followed to [6-11]. First, we determine channel potential by the solution of Poisson's equation including both types of doping; body doping and mobile charge concentrations of long channel surrounding-gate (SRG) devices with using appropriate boundary conditions. And, latter an expression of drain current is derived. The proposed model is verified by using simulation results [13].

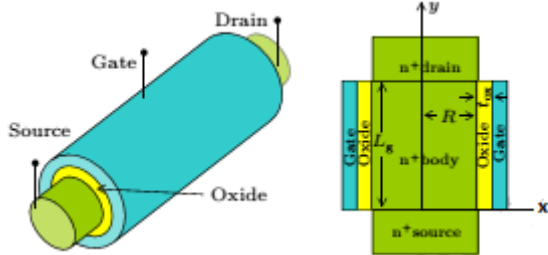


Fig.(a)

Fig. 1(b)

Expression of Channel Potential

Figures 1(a) and 1(b) are shown the 3-D structure of n-channel Silicon JL SRG MOSFET and cross section, respectively. The numerical analysis of the quantum effect verifies that the classical model is basically valid for a thickness of silicon body more than or equal to 5 nm. [9]. We suggest that the model derived in the following is suitable for a thickness of silicon body larger than mention above by solving Poisson Equation. Under gradual channel approximation, the channel potential of JL SRG MOSFET can be described by a Poisson–Boltzmann equation in the cylindrical coordinate

$$\frac{1}{r} \frac{d}{dr} \left(\frac{d\phi(r)}{dr} \right) = \frac{-qN_D}{\epsilon_{Si}} + \frac{qn_i}{\epsilon_{Si}} e^{q(\phi - V_{ch} - 2\phi_F)/KT} \quad (1)$$

where q is the electronic charge, ϵ_{Si} is the permittivity of Si, n_i is the intrinsic silicon electron concentration, K is the Boltzmann constant, T is absolute temperature, ϕ is the electrostatic potential, V_{ch} is quasi-Fermi potential and ϕ_F is the Fermi potential. The equation (1) must satisfies following boundary conditions

$$\left. \frac{d\phi(r)}{dr} \right|_{r=0} \text{ and } \phi(R) = \phi_s \quad (2)$$

Where R is the body radius, ϕ_s is the surface potential. Equation (1) contains both the depletion charge and mobile charge terms. But, to the extent our knowledge, there is no analytical solution for this equation. However, in the case of undoped or lightly doped, the solution of this equation can be analytically derived. To obtain the analytic channel potential for the highly doped case, we can deal with it using a kind of approximation method. To solve Equation (1), we take the solution of the undoped case as an initial guess, which is presented elsewhere [12, 14] as

$$\phi(r) = V_{ch} + 2\phi_F + \frac{KT}{q} \ln \left[\frac{8(1-\alpha)KT \epsilon_{Si}}{q^2 n_i (R^2 - (1-\alpha)r^2)} \right] \quad (3)$$

Where α is a constant whose value changes from source to drain. Substituting the equation (3) in equation (1), Poisson–Boltzmann's equation may be approximately expressed as

$$\frac{d^2 \phi(r)}{dr^2} + \frac{1}{r} \frac{d\phi(r)}{dr}$$

$$= \frac{q}{\epsilon_{Si}} \left[-N_D + \frac{8(1-\alpha)KT \epsilon_{Si}}{q^2 n_i (R^2 - (1-\alpha)r^2)} \right] \quad (4)$$

integrating equation (4) between the limit from $r = 0$ to $r = R$, the potential distributions along r direction, can be obtained as

$$\phi(r) = -\frac{q}{4\epsilon_{Si}} N_D r^2 - \frac{2KT}{q} \ln \left[1 - \frac{(1-\alpha)}{R^2} r^2 \right] + A \quad (5)$$

where A is an integral constant. The surface potential can be obtained from equation (5) as

$$\phi(R) = \phi_s = -\frac{q}{4\epsilon_{Si}} N_D R^2 - \frac{2KT}{q} \ln(\alpha) + A \quad (6)$$

An electric field at surface, on can obtain as

$$E_s = -\left. \frac{d\phi(r)}{dr} \right|_{r=R} = \frac{q}{2\epsilon_{Si}} N_D R - \frac{4KT(1-\alpha)}{qR\alpha} \quad (7)$$

The integral constant can be determined by the following boundary condition

$$C_{OX} = (V_{GS} - V_{FB} - \phi_s) = -\epsilon_{Si} E_s \quad (8)$$

where, V_{GS} is the gate--source voltage, $\Delta\phi$ is work function difference between gate material and semiconductor and C_{OX} is the gate oxide capacitance per unit area whose can be determine expressed as

$$C_{OX} = \frac{\epsilon_{OX}}{R \ln \left(1 + \frac{t_{OX}}{R} \right)} \quad (9)$$

substituting the equations (6), (7) and (9) into equation. (8), after solving, the integral A constant can

$$\text{be expressed as } A = qRN_D \left[\frac{R}{4\epsilon_{Si}} + \frac{1}{2C_{OX}} \right] + \frac{2KT}{q} \left[\ln(\alpha) - \frac{2\epsilon_{Si}(1-\alpha)}{R\alpha C_{OX}} \right] + V_{GS} - V_{FB} \quad (10)$$

the equation (10) shows that integral constant (A) is the function of " α ". Substituting equation (10) into equation (5), we have been obtained final expression of potential

$$\phi(r, \alpha) = \frac{qN_D}{4\epsilon_{Si}} \left[R^2 - r^2 + \frac{2\epsilon_{Si}R^2}{\epsilon_{OX}} \ln \left(1 + \frac{t_{OX}}{R} \right) \right] + \frac{2KT}{q} \ln \left[\frac{R^2 \alpha}{R^2 + (\alpha - 1)r^2} \right] - \frac{KT \epsilon_{Si} (1-\alpha)}{q\alpha \epsilon_{OX}} \ln \left(1 + \frac{t_{OX}}{R} \right) + V_{GS} - V_{FB} \quad (11)$$

Expression of Drain Current

The equation (11) is represented 2-dimensioninonal potential variation along r and α . From source to drain, we assume that the value of

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integral constant (α) shifts from α_s to α_D , therefore the drain-source current I_{DS} can be expressed a

$$I_{DS} = \frac{2\pi q \mu n_i \alpha_D}{L_{ch} \alpha_s} \int d\alpha \frac{d\phi_F}{d\alpha} \int_0^R re^{q(\phi - V_{ch} - 2\phi_F)/KT} dr \quad (12)$$

In order to determination drain-source current (I_{DS}), the relationship between integral constant (α) and quasi channel potential V_{ch} is derived by using following boundary condition

$$\epsilon_{Si} E_s = -(Q_D + Q_{in}) \quad (13)$$

Where Q_D and Q_{in} are the depletion charge density and the inversion charge density, respectively. The both charge densities can be determined by using following expressions

$$Q_D = \frac{qN_D R}{2} \quad (14)$$

$$Q_{in} = \frac{qn_i}{2\pi R} \int_0^{2\pi} \int_0^R re^{q(\phi - V_{ch} - 2\phi_F)/KT} dr \quad (15)$$

Substituting equations. (14), (15) and (7) into equation. (13), the quasi-Fermi potential approximately may be expressed as

$$V_{ch} = -\frac{KT}{q} \ln \left[\frac{4KT \epsilon_{Si} (1 - \alpha)}{q^2 n_i \alpha \int_0^R re^{q(\phi - 2\phi_F)/KT} dr} \right] \quad (16)$$

Using equation (16) into equation(12), drain-source current (I_{DS}), may be easily calculated of JL SRG MOSFET.

Results and Discussion

In the Fig.2 has been shown, that the channel potential increases non-linearly with the increasing channel depth for the different values of gate-source voltage. The Fig.3 shows that for different values of gate voltage, the drain-source current is seen to grow initially with the increasing V_{DS} and finally reaches saturation value. The saturation of I_{DS} occurs because most of the applied drain voltage is dropped in depletion region and not to induce the free carriers in the channel. The saturation current is seen to be more pronounced for higher values of doping concentration (N_D) because of reduction in the resistivity of channel.

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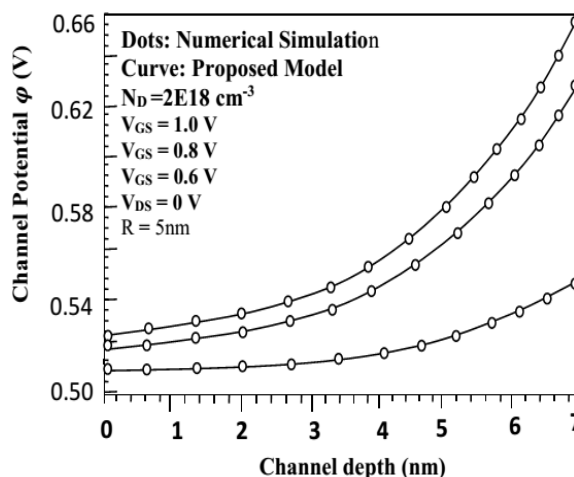


Fig.2 shows the variation in channel potential with channel depth for different values of gate-source voltage (V_{GS}).

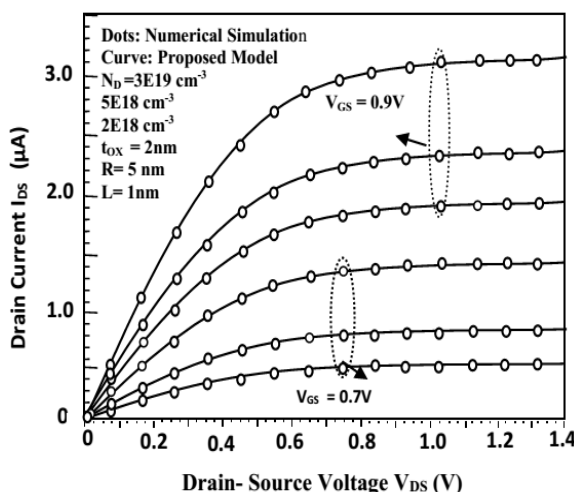
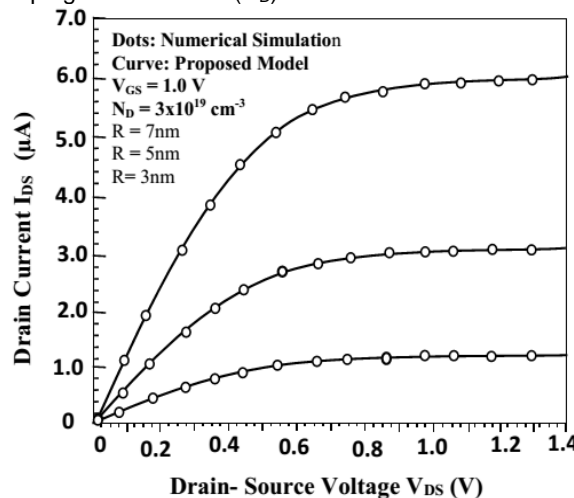


Fig.2 shows the variation in drain-source (I_{DS}) with drain-source voltage (V_{DS}) for different values of doping concentration (N_D).



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Fig.3 shows the variation in drain-source (I_{DS}) with drain-source voltage (V_{DS}) for different values of body radius (R).

The presented results are reasonably have good agreement with the simulation results. Fig.4 again shows the the dependency of drain-source (I_{DS}) on the drain-source voltage (V_{DS}) for different values of body radius (R). for large value of body radius the drain current is larger, because of large body radius device has more charge carriers than that of smaller body radius device

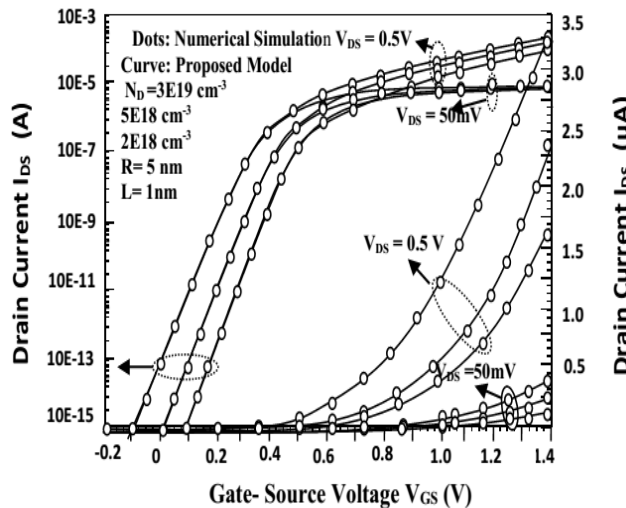


Fig.5 shows the variation in drain-source (I_{DS}) with gate-source voltage (V_{GS}) for different values of doping concentration (N_D).

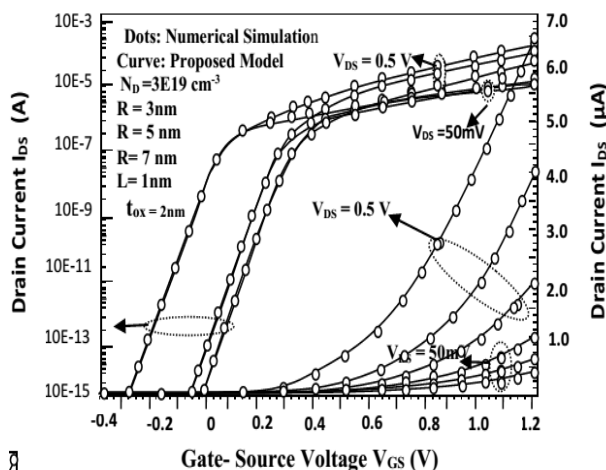


Fig.6 shows the variation in drain-source (I_{DS}) with gate-source voltage (V_{GS}) for different values of body radius (R).

In Figs.5 and 6, we compare the I_{DS} - V_{GS} curves between our results and the simulation results body doping and different radius of silicon body, respectively. The gate--source voltage is set to be 0.7V and 0.9V, respectively. In both linear and saturation regions, the proposed results matches well with the Atlas TCAD simulation results. Under the same gate-source voltage, for example, 0.7V and 0.9V, as shown in Fig.6 we can see that compared to the thinner body, the thicker body can induce more

Asian Resonance

current than that the thinner body. Because of reduction of channel resistivity with doping and improved conduction in the source and drain

Conclusion

On the basis an approximate solution of Poisson's-Boltzmann equation, compact continuous current model for accumulation mode Junctionless Silicon SRG MOSFETs without using any empirical fitting parameters and considering the effect such as, short channel effects, less degradation mobility with temperature small DIBL, role off threshold voltage and subthreshold swing has been presented. Finally the results are in the model have been verified by comparing with the simulation's result with various body doping concentrations and radius of silicon body. The results have reasonably good agreement with the numerical simulation data in all current operation regions, such as subthreshold, turn-on, linear, and saturation. It may be provide fundamentals for understanding accumulation mode junctionless SRG nanowire Si MOSFET.

References

1. Jin Xiao-Shi, Liu Xi, Kwon Hyuck-In and L EE Jong-Ho, "A Continuous Current Model of Accumulation Mode (Junctionless) Cylindrical Surrounding-Gate Nanowire MOSFETs", *Chin. Phys. Lett.*, 30, (3), 2013.
2. Lee C W, Afzalian A, Akhavan N D et al; "Junctionless multigate Field Effect Transistor", *Appl Phys Lett* 94 (5), 2009.
3. Keng-Ming Liu et al; "The effects of channel doping concentration for n-type junction-less double-gate poly-Si nanowire transistors", *Semiconductor Science and Technology*, 29(5), 2014
4. Punyasloka Bal, Bahniman Ghosh et al; "A laterally graded junctionless transistor", *Journal of Semiconductors*, 35(3), 2014.
5. Renan Doria Trevisoli et al; "Threshold voltage in junctionless nanowire transistors", *Semiconductor Science and Technology*, 26 (10), 2011.
6. Mu-Shih Yeh et al; "A single poly-Si gate-all-around junctionless fin field-effect transistor for use in one-time programming nonvolatile memory", 9(1), 2014.
7. Colinge J P et al ; "Nanowire transistors without junctions", *Nat Nanotechnol* 5(3), 2010.
8. Park C H et al; "Electrical Characteristics of 20 nm Junctionless Si Nanowire Transistors" *Solid State Electronics* 73(7), 2012.
9. Masanari Shoji and Seiji Horiguchi; "Electronic structures and phonon-limited electron mobility of double-gate silicon-on-insulator Si inversion layers", *Journal of Applied Physics* 85 (5), 1999.
10. Hiroyuki Kageshima and Akira Fujiwara; "First-principles study on inversion layer properties of double-gate atomically thin silicon channels", *Journal of Applied Physics* 93(4), 2008.
11. Himangi Sood, Viranjay M. Srivastava, and Ghanshyam Singh "Advanced MOSFET Technologies for Next Generation Communication Systems-Perspective and Challenges", *Journal of Engineering Science and Technology*, 11 (3) 2018.

E: ISSN No. 2349-9443

12. YV Bhuvaneshwari and Abhinav Kranti, "Estimation of doping in junctionless transistors through dc characteristics", *semiconductor science and Technology*, 5 (14), 2019
13. Silvaco O 2007 International 2007 ATLAS User's Manual [http://www.silvaco.com/products/device simulation/atlas.html](http://www.silvaco.com/products/device_simulation/atlas.html).
14. D. Jimenez et al; "Continuous analytic I-V model for surrounding-gate MOSFETs", *IEEE Electron Device Lett.* ,25 (8), 2004